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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/723.965

11/26/2003

Fujio Takeda

SIG000116

9518

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7590

07/12/2006

GARLICK HARRISON & MARKISON

P.O. BOX 160727

AUSTIN, TX 78716-0727

EXAMINER

NGUYEN, DANNY

ART UNIT

PAPER NUMBER

2836

DATE MAILED: 07/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/723,965

Applicant(s)

TAKEDA, FUJIO

Examiner

Danny Nguyen

Art Unit

2836

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 25 April 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-4, 6, 7, 9-12, 14, 15 is/are rejected.
- 7) ☒ Claim(s) 5, 8, 13 and 16 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1 and 9 have been considered but are moot in view of the new ground(s) of rejection.

The indicated allowability of claims 6, 7, 14, and 15 are withdrawn in view of the newly discovered reference(s) to Young et al (USPN 5,978,192). Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Miller (USPN 5,255,146).

Regarding claims 1, 2, Miller discloses an ESD protection circuit (figures 1, 2, 5) comprises ESD clamping circuit (16) operably coupled to a first power pin (10a) and a second power pin (12a) of the integrated circuit (see figure 2), ESD triggering circuit (22, 30, 50) operably coupled to the clamping circuit, wherein, when enabled and when sensing an ESD event, the triggering circuit provides a clamping signal to the clamping circuit such that the clamping circuit provides a low impedance path between the first and second power pins, the ESD triggering circuit having a first time response to sense the ESD event (col. 4, lines 14-22), and a second time response for the clamping signal

to activate the clamping circuit, in which the first time response is different than the second time response (col. 4, lines 50-56), ESD disabling circuit (24, 40) operably coupled to disable the triggering circuit when the integrated circuit is in a normal operation mode (see abstract).

Regarding claim 3, Miller discloses the triggering circuit comprises an ESD sensing module (30) senses the ESD event and provides a corresponding sensed voltage signal (S) based on the first time response, and a timed latch module (22, 50) receive the sensed signal and provides the clamping signal for a given duration on the second time response.

Regarding claim 4, Miller discloses the ESD sensing module comprises a capacitor (30, see figure 5) having a first node and a second node, wherein the first node of the capacitor is operably coupled to a pin of the integrated circuit that is susceptible to the ESD event; and a resistor (32) having a first node and a second node, wherein the second node of the resistor is coupled to the first power pin of the integrated circuit and the first node of the resistor is coupled to the second node of the capacitor to provide the corresponding sensed voltage, and wherein a time constant of the resistor and the capacitor determines the first time response and is greater than a rise time of the ESD event, is less than a rise time of a power supply of the integrated circuit, and is independent of the given duration of the second time response provided by the time latched module (col. 4, lines 14-22, 50-56).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claim 6, 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller in view of Young et al (USPN 5,978,192). Miller discloses all limitations of claim 1 as discussed above, but Miller does not disclose a first diode and a second diode as claimed. Young discloses an ESD protection circuit for an integrated circuit (figure 1) comprises first and second diodes (D1 and D2), wherein the first diode (D1) coupled to input pin or the output pin to the first power supply (Vdd), the second diode (D2) coupled to the input pin or the output pin to the second power supply (Vss). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the integrated circuit of Miller to incorporate the diodes in order to protection the integrated circuit from a transient voltage event.

4. Claims 9-12, 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Grassian (PN 20040083315) in view of Miller. Grassian discloses an integrated circuit of use in a multiple function handheld device, wherein the integrated circuit comprises a processing module (20) operably coupled to perform at least one algorithm (30) relating to a function of the multiple function handheld device (0011); a multimedia module (24) operably coupled to produce rendered output data from data corresponding to the processing of the at least one algorithm by the processing module; at least one input pin operably coupled to the processing module; at least one output pin operably coupled to

the multimedia module. Grassian does not disclose an ESD protection circuitry as claimed. Miller discloses an integrated circuit (see figures 1, 2, 5) comprises ESD clamping circuit (16) operably coupled to a first power pin (10a) and a second power pin (12a) of the integrated circuit (see figure 2), ESD triggering circuit (22, 30, 50) operably coupled to the clamping circuit, wherein, when enabled and when sensing an ESD event, the triggering circuit provides a clamping signal to the clamping circuit such that the clamping circuit provides a low impedance path between the first and second power pins, the ESD triggering circuit having a first time response to sense the ESD event (col. 4, lines 14-22), and a second time response for the clamping signal to activate the clamping circuit, in which the first time response is different than the second time response (col. 4, lines 50-56), ESD disabling circuit (24, 40) operably coupled to disable the triggering circuit when the integrated circuit is in a normal operation mode (see abstract). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the integrated circuit of Grassian to incorporate the ESD protection circuitry as disclosed by Miller in order to protect the integrated circuit from an ESD event.

5. Claims 14, 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Grassian in view of Miller, and Young et al (USPN 5,978,192). Grassian and Miller disclose all limitations of claim 9 as discussed above, but do not disclose a first diode and a second diode as claimed. Young discloses an ESD protection circuit for an integrated circuit (figure 1) comprises first and second diodes (D1 and D2), wherein the first diode (D1) coupled to input pin or the output pin to the first power supply (Vdd), the

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second diode (D2) coupled to the input pin or the output pin to the second power supply (Vss). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the integrated circuit of Grassian and Miller to incorporate the diodes in order to protection the integrated circuit from a transient voltage event.

Allowable Subject Matter

6. Claims 5, 8, 13, 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

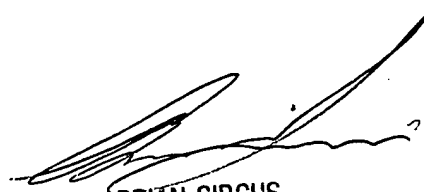
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Danny Nguyen whose telephone number is (571)-272-2054. The examiner can normally be reached on Mon to Fri 8:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571)-272-2058. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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7/6/2006



BRIAN SIRCUS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800